IN THE CLAIMS

1-24. (Canceled)

25. (Currently Amended) A processor comprising:

an execution unit including

a first parity-protected storage structure having a first parity bit and

a second parity-protected storage structure having a second parity bit;

a check unit coupled to the first parity-protected storage structure and the second parity-protected storage structure, the check unit to monitor the ~~the~~ first parity-protected storage structure and the second parity-protected storage structure, to detect a parity error in data accessed from the first parity-protected storage structure or in data accessed from the second parity-protected storage structure, and to signal a parity error; and

a replay queue coupled to the check unit and the execution unit, the at least one replay queue to issue a plurality of instructions to the protected execution unit for processing, to track the plurality of instructions issued to the protected execution unit, and to selectively reissue one or more of the plurality of instructions to the protected execution unit in response to the check unit detecting and signaling a parity error.

26. (Previously Presented) The processor of claim 25, wherein

a parity error indicates a soft error corrupted data after it was stored into the first parity-protected storage structure or the second parity-protected storage structure.

27. (Previously Presented) The processor of claim 25, wherein

the first parity-protected storage structure is a register file to store a first plurality of data blocks each of which has a first parity bit, and

the second parity-protected storage structure is a cache to store a second plurality of data blocks each of which has a second parity bit.

28. (Previously Presented) A processor comprising:

an execution unit including

a first protected storage structure having a first plurality of error correction control bits;

a second protected storage structure having a second plurality of error correction control bits;

a check unit coupled to the first parity-protected storage structure and the second parity-protected storage structure, the check unit to monitor the first protected storage structure and the second protected storage structure, to detect an error in data accessed from the first protected storage structure or in data accessed from the second protected storage structure, and to correct the error in the accessed data in response to the first or second plurality of error correction control bits, respectively; and

a replay queue coupled to the check unit and the execution unit, the at least one replay queue to issue a plurality of instructions to the protected execution unit for processing, to track the plurality of instructions issued to the protected execution unit, and to selectively reissue one or more of the plurality of instructions to the protected execution unit in response to the check unit detecting an error in instruction execution.

29. (Previously Presented) The processor of claim 28, wherein

the first protected storage structure is a register file to store a first plurality of data blocks each of which has a first plurality of error correction bits, and

the second protected storage structure is a cache to store a second plurality of data blocks each of which has a second plurality of error correction bits.

30.-33. (Canceled)